N-Channel JFETs

**PRODUCT SUMMARY**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>$V_{GS\text{off}}$ (V)</th>
<th>$V_{(BR)GSS\text{Min}}$ (V)</th>
<th>$g_{fs\text{Min}}$ (mS)</th>
<th>$I_{DSS\text{Min}}$ (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2N4416</td>
<td>$\leq 6$</td>
<td>$-30$</td>
<td>4.5</td>
<td>5</td>
</tr>
<tr>
<td>2N4416A</td>
<td>$-2.5$ to $-6$</td>
<td>$-35$</td>
<td>4.5</td>
<td>5</td>
</tr>
<tr>
<td>SST4416</td>
<td>$\leq 6$</td>
<td>$-30$</td>
<td>4.5</td>
<td>5</td>
</tr>
</tbody>
</table>

**FEATURES**

- Excellent High-Frequency Gain: $2N4416/A$, $G_{ps}$ 13 dB (typ) @ 400 MHz
- Very Low Noise: 3 dB (typ) @ 400 MHz
- Very Low Distortion
- High AC/DC Switch Off-Isolation

**BENEFITS**

- Wideband High Gain
- Very High System Sensitivity
- High Quality of Amplification
- High-Speed Switching Capability
- High Low-Level Signal Amplification

**APPLICATIONS**

- High-Frequency Amplifier/Mixer
- Oscillator
- Sample-and-Hold
- Very Low Capacitance Switches

**DESCRIPTION**

The 2N4416/2N4416A/SST4416 n-channel JFETs are designed to provide high-performance amplification at high frequencies. The TO-206AF (TO-72) hermetically-sealed package is available with full military processing (see Military Information.) The TO-236 (SOT-23) package provides a low-cost option and is available with tape-and-reel options (see Packaging Information). For similar products in the TO-226AA (TO-92) package, see the J304/305 data sheet.
2N4416/2N4416A/SST4416
Vishay Siliconix

ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage :
(2N/SST4416)  −30 V
(2N4416A)  −35 V
Gate Current 10 mA
Lead Temperature 300 °C
Storage Temperature :
(2N Prefix)  −65 to 200 °C
(SST Prefix)  −65 to 150 °C
Operating Junction Temperature −55 to 150 °C
Power Dissipation :
(2N Prefix)a 300 mW
(SST Prefix)b 350 mW

Notes
a. Derate 2.4 mW/°C above 25 °C
b. Derate 2.8 mW/°C above 25 °C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (TA = 25 °C UNLESS NOTED)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Typa</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate-Source Breakdown Voltage</td>
<td>V(BR)GSS</td>
<td>IG = −1 μA, VDS = 0 V</td>
<td>−36 −30 −35 −30</td>
</tr>
<tr>
<td>Gate-Source Cutoff Voltage</td>
<td>VGS(off)</td>
<td>VDS = 15 V, ID = 1 nA</td>
<td>−3 −6 −2.5 −6 −6</td>
</tr>
<tr>
<td>Saturation Drain Currentb</td>
<td>IDSS</td>
<td>VDS = 15 V, VGS = 0 V</td>
<td>10 5 15 5 15 5 mAh</td>
</tr>
<tr>
<td>Gate Reverse Current</td>
<td>IDSS</td>
<td>VGS = −20 V, VDS = 0 V (2N)</td>
<td>−2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VGS = −15 V, VDS = 0 V (SST)</td>
<td>−0.002</td>
</tr>
<tr>
<td>Gate Operating Current</td>
<td>IG</td>
<td>VDS = 10 V, ID = 1 mA</td>
<td>−20</td>
</tr>
<tr>
<td>Drain Cutoff Currentc</td>
<td>ID(off)</td>
<td>VDS = 10 V, VGS = −6 V</td>
<td>2</td>
</tr>
<tr>
<td>Drain-Source On-Resistancec</td>
<td>rDSS(on)</td>
<td>VGS = 0 V, ID = 300 μA</td>
<td>150</td>
</tr>
<tr>
<td>Gate-Source Forward Voltagec</td>
<td>VGS(F)</td>
<td>IG = 1 mA, VDS = 0 V</td>
<td>0.7</td>
</tr>
</tbody>
</table>

Dynamic

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common-Source Forward Transconductanceb</td>
<td>gfs</td>
<td>VDS = 15 V, VGS = 0 V</td>
<td>6 4.5 7.5 4.5 7.5 4.5 7.5 mS</td>
</tr>
<tr>
<td>Common-Source Output Conductanceb</td>
<td>gds</td>
<td>VDS = 15 V, VGS = 0 V</td>
<td>15 50 50 50 μS</td>
</tr>
<tr>
<td>Common-Source Input Capacitance</td>
<td>Ciss</td>
<td>VDS = 15 V, VGS = 0 V</td>
<td>2.2 4 4 pF</td>
</tr>
<tr>
<td>Common-Source Reverse Transfer Capacitance</td>
<td>Crss</td>
<td>VDS = 15 V, VGS = 0 V</td>
<td>0.7 0.8 0.8</td>
</tr>
<tr>
<td>Common-Source Output Capacitance</td>
<td>Coss</td>
<td>VDS = 10 V, VGS = 0 V</td>
<td>1 2 2</td>
</tr>
<tr>
<td>Equivalent Input Noise Voltagec</td>
<td>en</td>
<td>VDS = 10 V, VGS = 0 V</td>
<td>6 nV/√Hz</td>
</tr>
</tbody>
</table>
HIGH-FREQUENCY SPECIFICATIONS FOR 2N4416/2N4416A (T_A = 25°C UNLESS NOTED)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>100 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
</tr>
<tr>
<td>Common Source Input Conductance(^d)</td>
<td>giss</td>
<td>V_DS = 15 V, V_GS = 0 V</td>
<td>100</td>
</tr>
<tr>
<td>Common Source Input Susceptance(^d)</td>
<td>bis</td>
<td>V_DS = 15 V, V_GS = 0 V</td>
<td>2,500</td>
</tr>
<tr>
<td>Common Source Output Conductance(^d)</td>
<td>goss</td>
<td>V_DS = 15 V, V_GS = 0 V</td>
<td>75</td>
</tr>
<tr>
<td>Common Source Output Susceptance(^d)</td>
<td>boss</td>
<td>V_DS = 15 V, V_GS = 0 V</td>
<td>1,000</td>
</tr>
<tr>
<td>Common Source Forward Transconductance(^d)</td>
<td>gfs</td>
<td>V_DS = 10 V, V_GS = 0 V</td>
<td>1,000</td>
</tr>
<tr>
<td>Common-Source Power Gain(^d)</td>
<td>Gps</td>
<td>V_DS = 15 V, I_D = 5 mA</td>
<td>18</td>
</tr>
<tr>
<td>Noise Figure(^d)</td>
<td>NF</td>
<td>R_G = 1 kΩ</td>
<td>2</td>
</tr>
</tbody>
</table>

Notes:

a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.c. This parameter not registered with JEDEC.
d. Not a production test.

TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)
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Output Characteristics

Transfer Characteristics

Transconductance vs. Gate-Source Voltage
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C UNLESS OTHERWISE NOTED}$)

- **On-Resistance vs. Drain Current**: Graph showing $r_{DS(on)}$ vs. $I_D$.
  - $T_A = 25^\circ\text{C}$.
  - $V_{GS(th)} = -2$ V.
  - $V_{GS(th)} = -3$ V.

- **Circuit Voltage Gain vs. Drain Current**: Graph showing $A_V$ vs. $I_D$.
  - $A_V = \frac{g_{fs}}{1 + \frac{g_{fs}}{R_L}}$.
  - Assume $V_{DD} = 15$ V, $V_{DS} = 5$ V.

- **Common-Source Input Capacitance vs. Gate-Source Voltage**: Graph showing $C_{iss}$ vs. $V_{GS}$.
  - $f = 1$ MHz.
  - $V_{DS} = 0$ V.

- **Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage**: Graph showing $C_{rss}$ vs. $V_{GS}$.
  - $f = 1$ MHz.
  - $V_{DS} = 0$ V.

- **Input Admittance**: Graph showing $I_{ds}$ vs. $f$.
  - $T_A = 25^\circ\text{C}$.
  - $V_{DS} = 15$ V.
  - $V_{GS} = 0$ V.

- **Forward Admittance**: Graph showing $g_{fs}$ vs. $f$.
  - $T_A = 25^\circ\text{C}$.
  - $V_{DS} = 15$ V.
  - $V_{GS} = 0$ V.
TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

Reverse Admittance

Output Admittance

Gate Leakage Current

Common-Source Forward Transconductance vs. Drain Current

Equivalent Input Noise Voltage vs. Frequency

Output Conductance vs. Drain Current

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