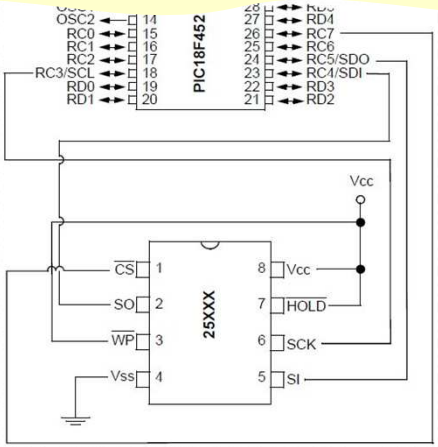
Le Bus S.P.I

Serial Peripheral Interface

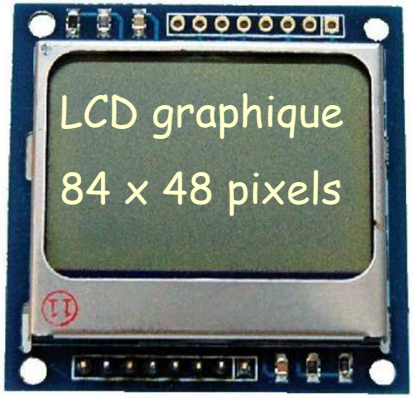
- Bus de communication entre circuits
- Mode série synchrone
- Fonctionnement en mode full duplex
- De type maître / esclave
- Pas de contrôle des données ni de contrôle de flux.

Applications du bus SPI

Mémoire EEPROM, FLASH..

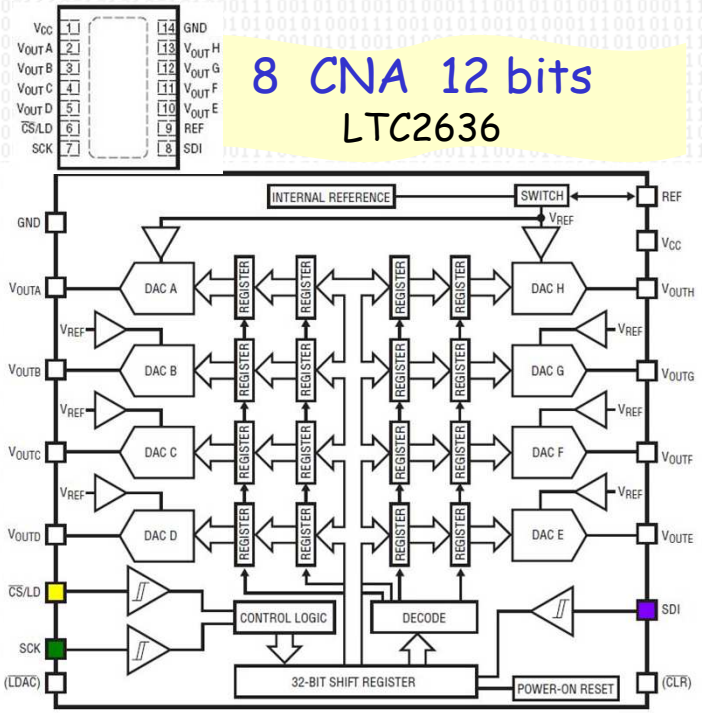


Afficheur LCD



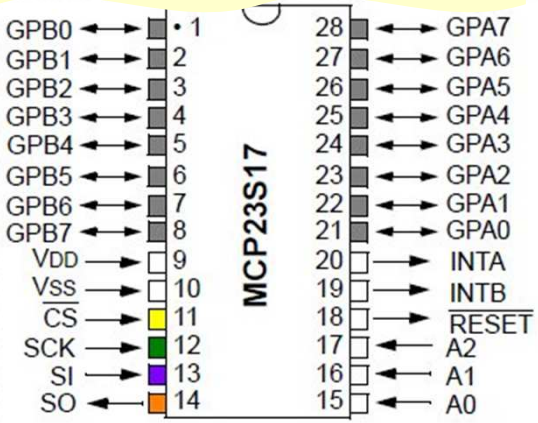
8 CNA 12 bits

LTC2636

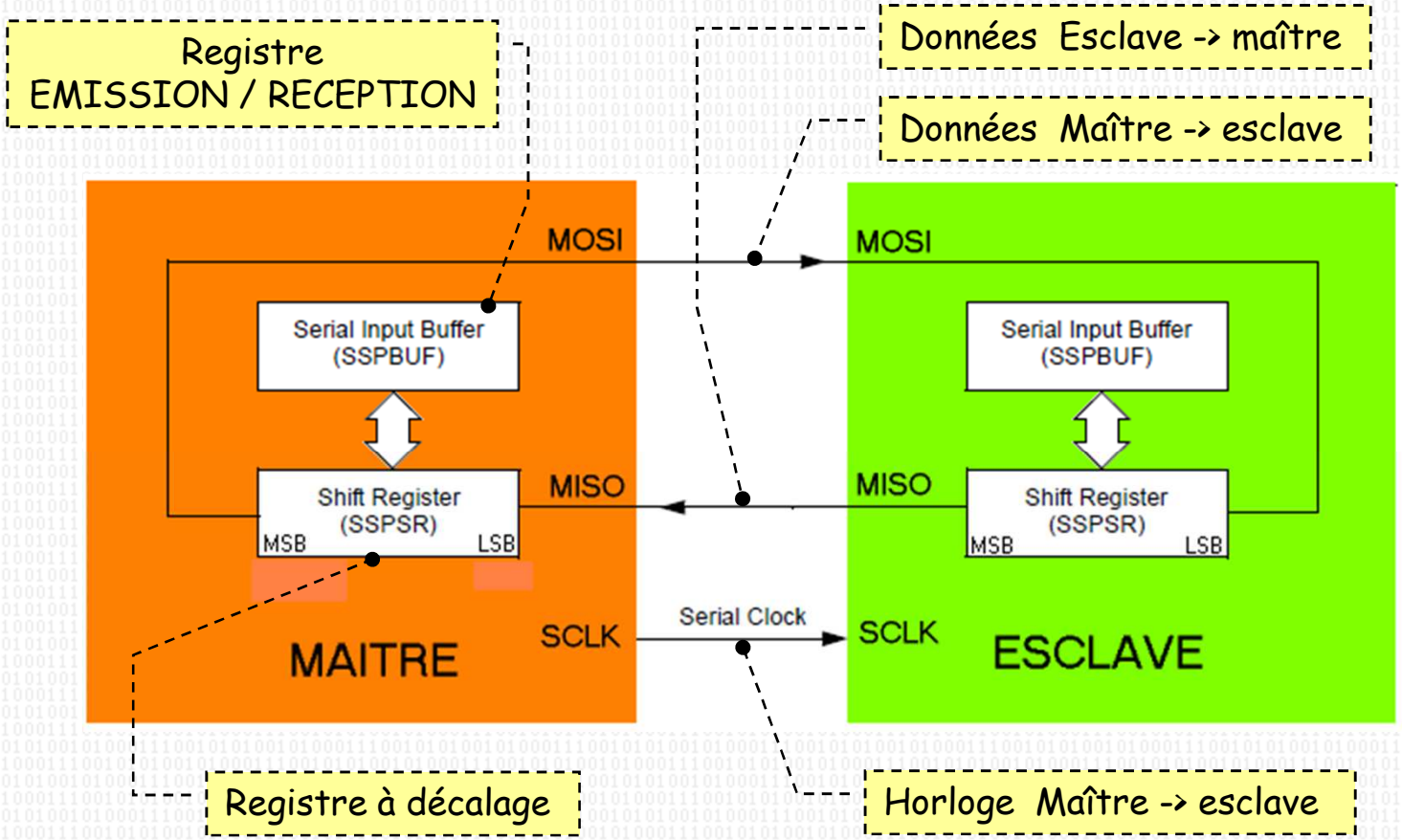


Extension de bus

2 x 8 bits



Bus SPI : Principe



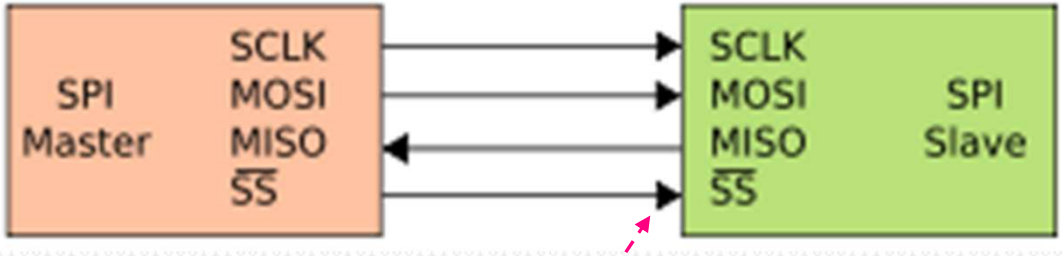
Bus SPI : les signaux

L'interface SPI spécifie 4 signaux :

- SCLK (clock)
  - horloge
- MOSI (master output, slave input)
  - sortie donnée maître, entrée donnée esclave
- MISO (master input, slave output)
  - entrée donnée maître, sortie donnée esclave
- SS (slave select)
  - sélection esclave

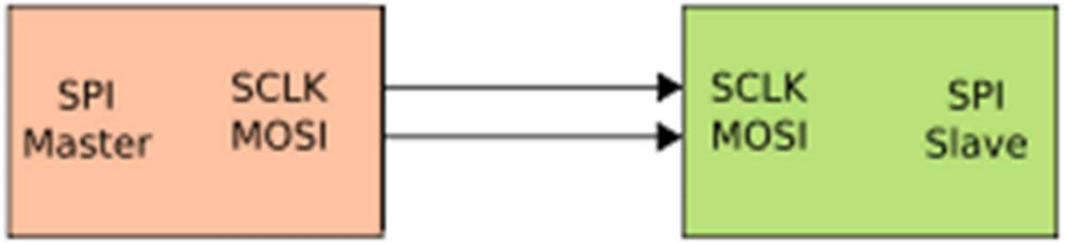
Bus SPI : câblage

Un seul esclave 4 signaux



Sélection esclave
Optionnel

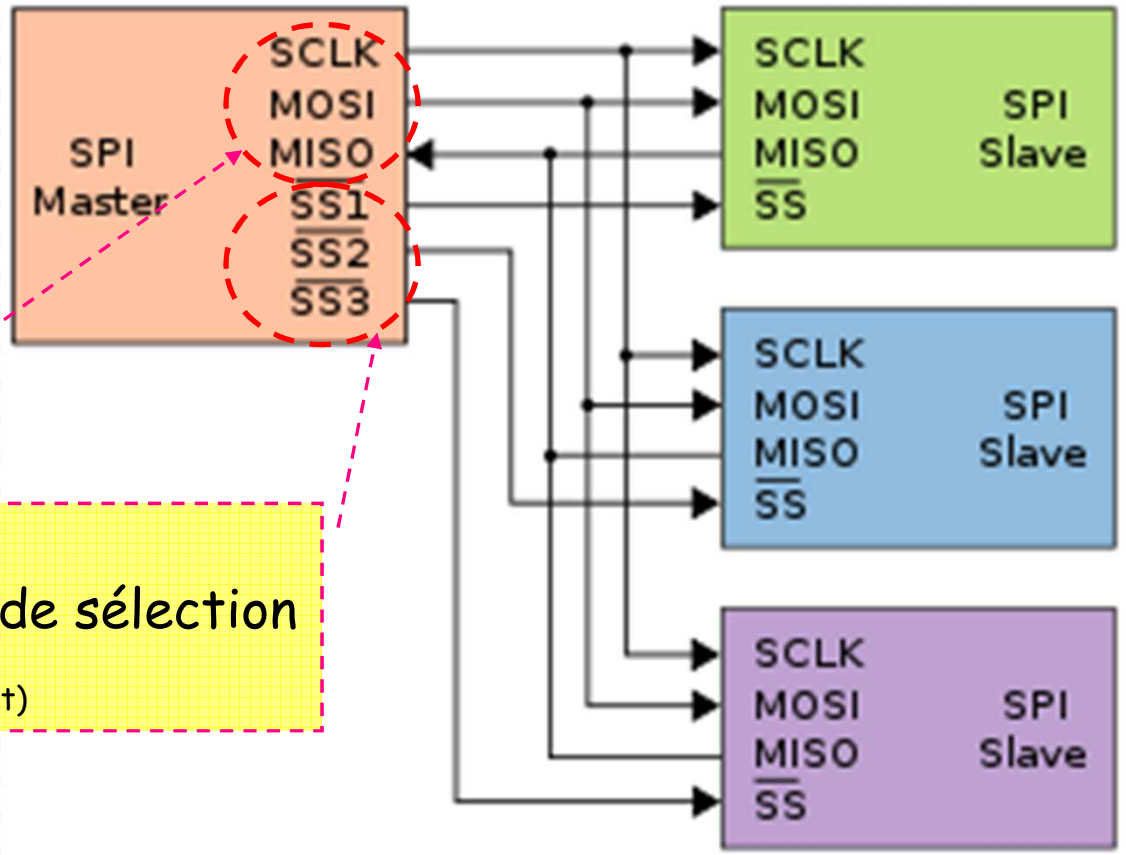
Un seul esclave câblage minimum



Bus SPI : câblage

Un seul esclave actif à la fois

Plusieurs esclaves



Signaux du bus

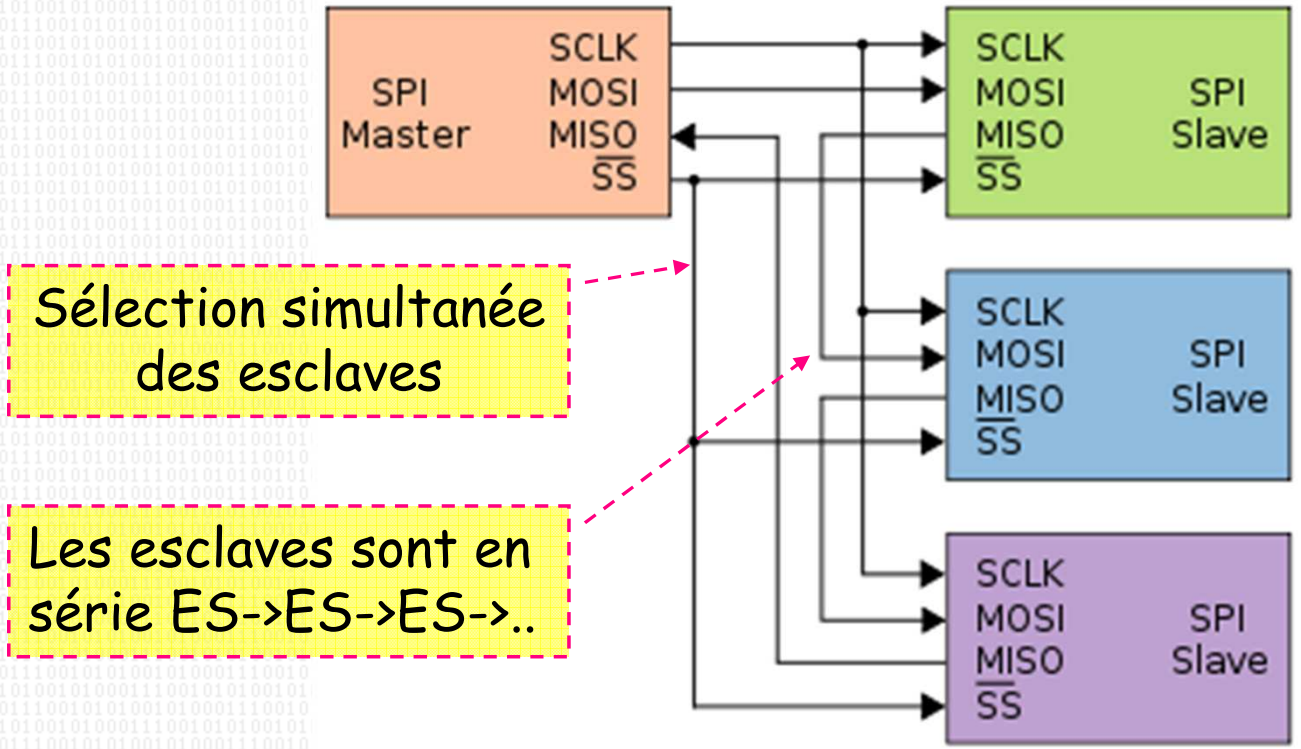
3 esclaves =
3 signaux de sélection

(SS = Slave Select)

Bus SPI : câblage

Plusieurs esclaves en ***daisy chain***

- Guirlande
- Cascade
- Série
- ……



Sélection simultanée des esclaves

Les esclaves sont en série ES->ES->ES->..

Le signal d 'horloge 1 / 2

Trois paramètres :

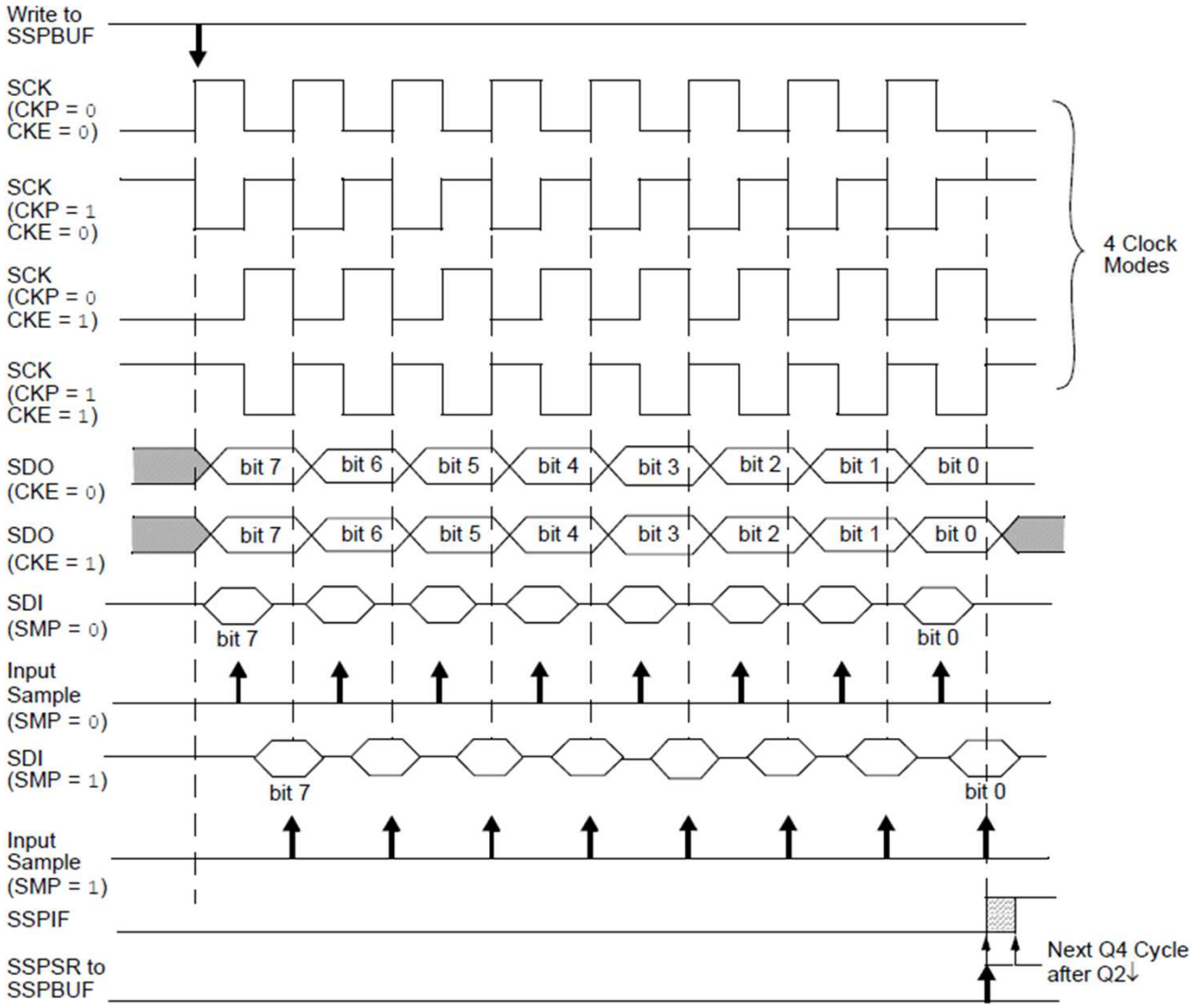
- La fréquence d'horloge.
- La polarité de l'horloge, paramètre CPOL (Clock polarity)
- La phase de l'horloge, paramètre CPHA (Clock phase).

SPI-mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

- CPOL et CPHA ont deux état possible :
  ⇒ 4 possibilités de configuration.
- Les configurations étant incompatibles entre elles :
  ⇒ Maître et esclave doivent avoir les mêmes paramètres.

- La fréquence de l 'horloge est fixée par le maître :
  ⇒ Elle doit tenir compte des possibilités de l 'esclave.
  ⇒ Pas de contrainte sur la précision.

Le signal d 'horloge



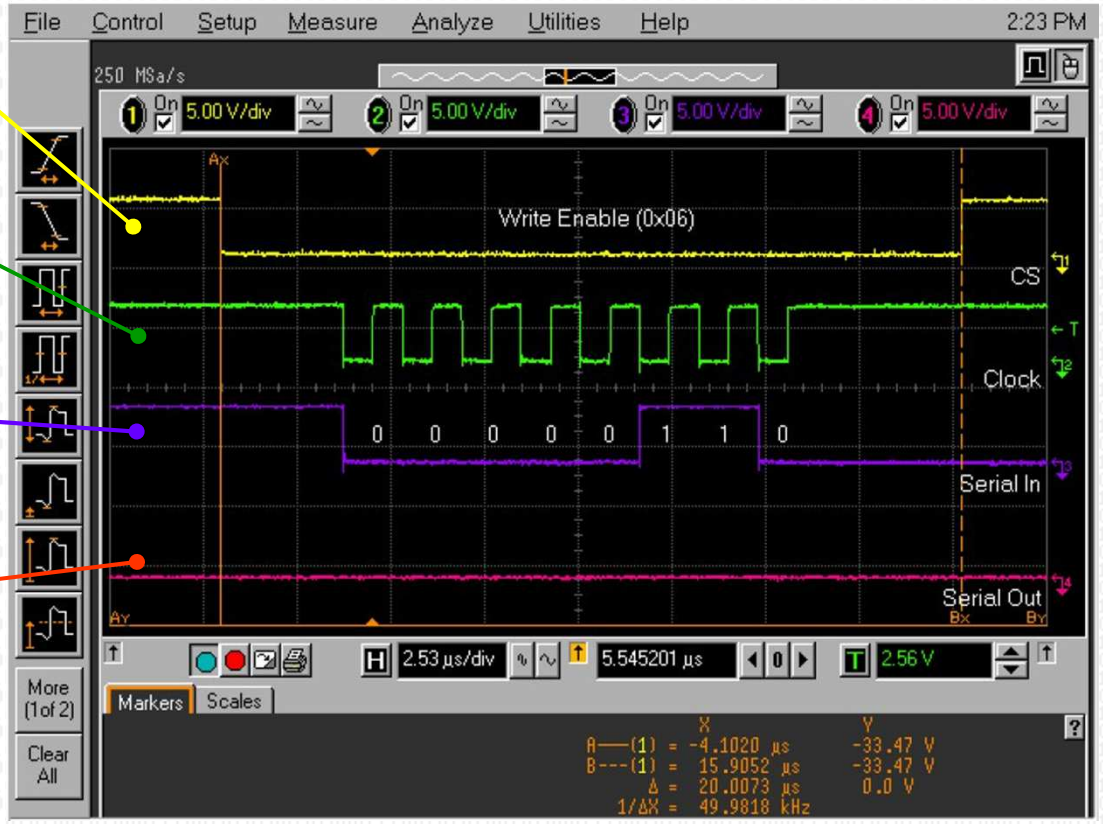
Signaux sur le bus SPI

Sélection
-CS = 0

Horloge
-Sur front ↗

µC -> 00000110
-Le MSB en premier

Sortie EEPROM
-En haute impédance



Exemple : autorisation d 'écriture dans une EEPROM

Signaux sur le bus SPI

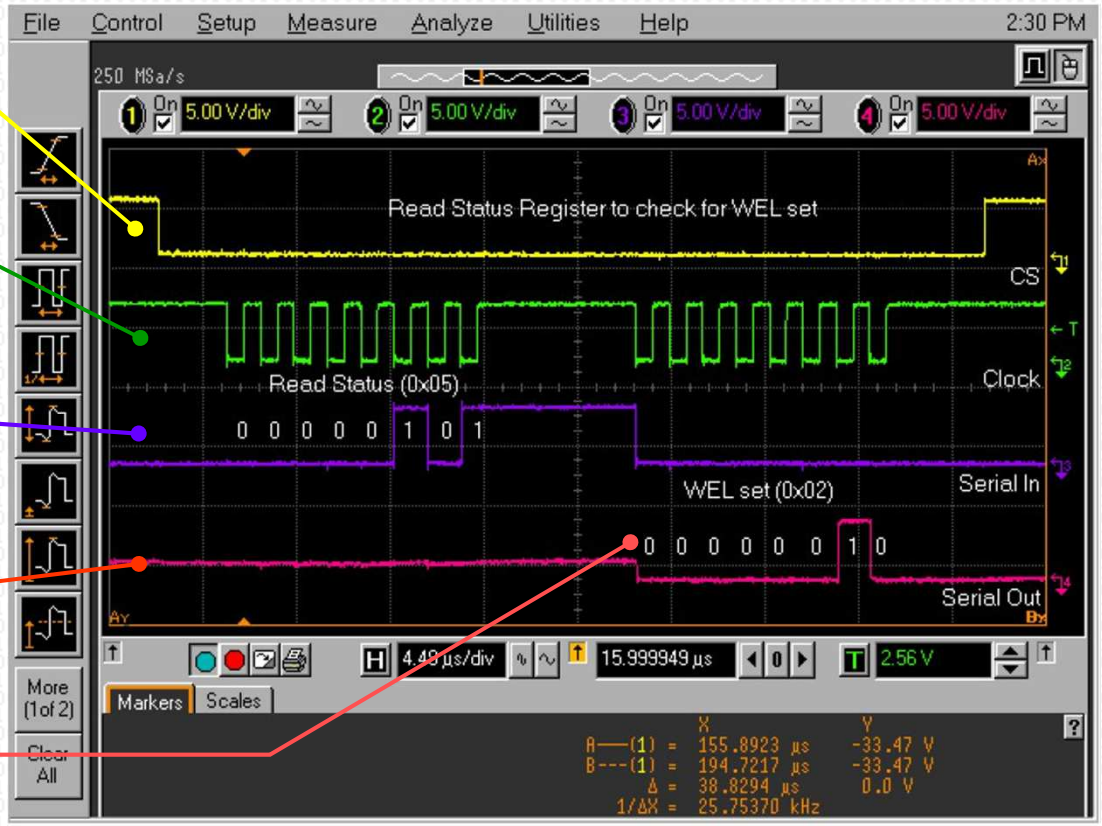
Sélection
-CS = 0

Horloge
-Sur front ↗

µC -> 00000101
-Le MSB en premier

Sortie EEPROM
-En haute impédance

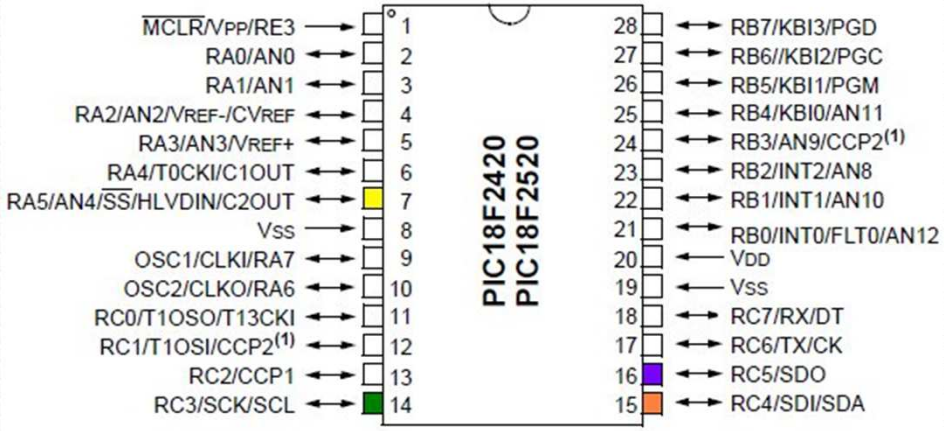
EEPROM-> 00000010
-Le MSB en premier



Exemple : lecture du registre d'état d 'une EEPROM

Les registres SPI du PIC

Boîtier DIP28



Le SPI dispose de 4 registres :

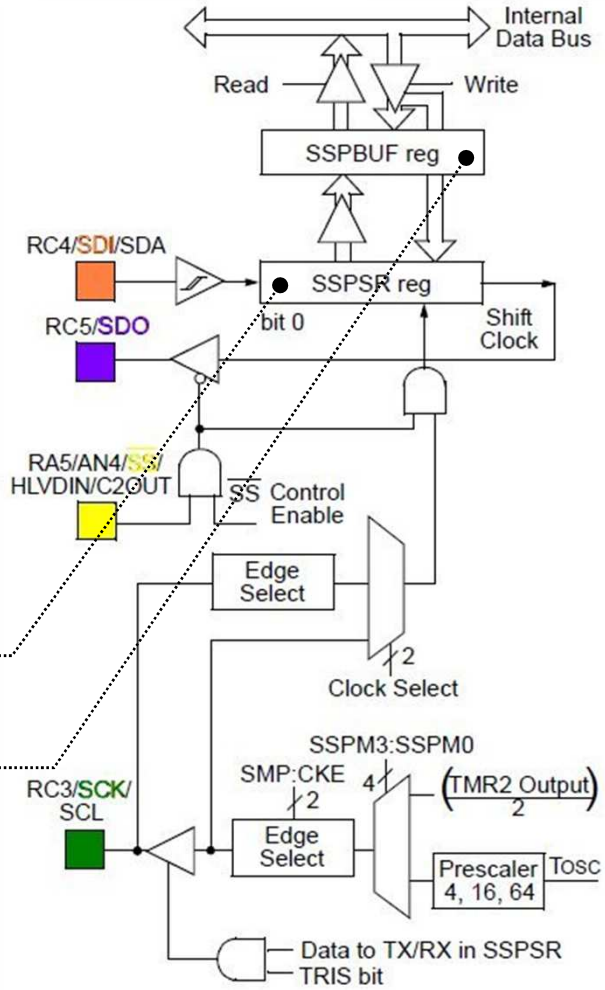
SSPSR : non accessible directement.

SSPBUF : pour lire et écrire les données

SSPCON1 : registre de contrôle

SSPSTAT : registre d 'état

MSSP BLOCK DIAGRAM (SPI MODE)



Les registres SPI du PIC

REGISTER 17-1: SSPSTAT: MSSP STATUS REGISTER (SPI MODE)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE(1)	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **SMP:** Sample bit
SPI Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
SPI Slave mode:
SMP must be cleared when SPI is used in Slave mode.

bit 6 **CKE:** SPI Clock Select bit(1)
1 = Transmit occurs on transition from active to Idle clock state
0 = Transmit occurs on transition from Idle to active clock state

bit 5 **D/$\overline{A}$:** Data/$\overline{Address}$ bit
Used in I^2C mode only.

bit 4 **P:** Stop bit
Used in I^2C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.

bit 3 **S:** Start bit
Used in I^2C mode only.

bit 2 **R/$\overline{W}$:** Read/$\overline{Write}$ Information bit
Used in I^2C mode only.

bit 1 **UA:** Update Address bit
Used in I^2C mode only.

bit 0 **BF:** Buffer Full Status bit (Receive mode only)
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty

Note 1: Polarity of clock state is set by the CKP bit (SSPCON1<4>).

REGISTER 17-2: SSPCON1: MSSP CONTROL REGISTER 1 (SPI MODE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV(1)	SSPEN(2)	CKP	SSPM3(3)	SSPM2(3)	SSPM1(3)	SSPM0(3)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **WCOL:** Write Collision Detect bit
1 = The SSPxBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

bit 6 **SSPOV:** Receive Overflow Indicator bit(1)
SPI Slave mode:
1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow (must be cleared in software).
0 = No overflow

bit 5 **SSPEN:** Master Synchronous Serial Port Enable bit(2)
1 = Enables serial port and configures SCK, SDO, SDI and $\overline{SS}$ as serial port pins
0 = Disables serial port and configures these pins as I/O port pins

bit 4 **CKP:** Clock Polarity Select bit
1 = Idle state for clock is a high level
0 = Idle state for clock is a low level

bit 3-0 **SSPM3:SSPM0:** Master Synchronous Serial Port Mode Select bits(3)
0101 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control disabled, $\overline{SS}$ can be used as I/O pin
0100 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control enabled
0011 = SPI Master mode, clock = TMR2 output/2
0010 = SPI Master mode, clock = Fosc/64
0001 = SPI Master mode, clock = Fosc/16
0000 = SPI Master mode, clock = Fosc/4

Note 1: In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.
2: When enabled, these pins must be properly configured as input or output.
3: Bit combinations not specifically listed here are either reserved or implemented in I^2C™ mode only.

Le Bus SPI
fin de transmission ...